Lecture – 4

8085 Pin Diagram

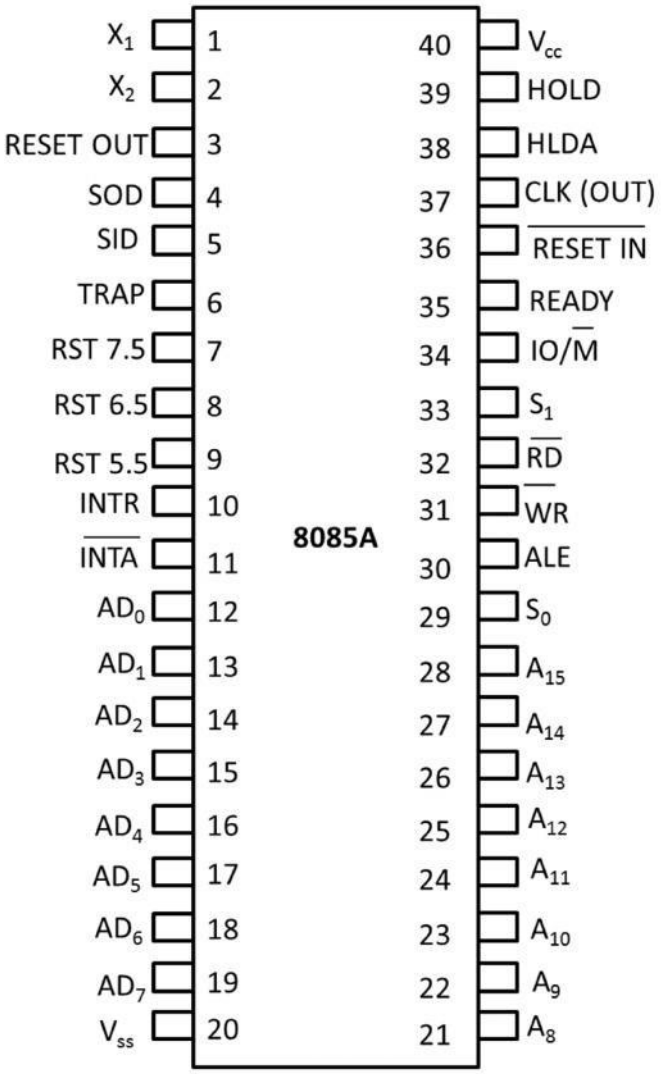

Figure: 8085 Pin Diagram

All signals can be classified into six groups:

1. Address Bus
2. Data Bus
3. Control & Status Signals
4. Power Supply & Frequency signals
5. Externally initiated signals

6. Serial I/O Ports

1) Address Bus (pin 12 to 28)

- 16 signal lines are used as address bus.
- However these lines are split into two segments: A_{15} - A_8 and AD_7 - AD_0
- A_{15} - A_8 are unidirectional and are used to carry high-order address of 16-bit address.
- AD_7 - AD_0 are used for dual purpose.

2) Data Bus/ Multiplexed Address (pin 12 to 19)

- Signal lines AD7-AD0 are bidirectional and serve dual purpose.
- They are used as low-order address bus as well as data bus.
- The low order address bus can be separate from these signals by using a latch.

3) Control & Status Signals

- To identify nature of operation
- Two Control Signals
  1) RD' (Read-pin 32)
     - ✓ This is a read control signal (active low)
     - ✓ This signal indicates that the selected I/O or Memory device is to be read & data are available on data bus.
  2) WR' (Write-pin 31)
     - ✓ This is a write control signal (active low)
     - ✓ This signal indicates that the selected I/O or Memory device is to be write.
- Three Status Signals
  1) S_1 (pin 33)
  2) S_0 (pin 29)
     - ✓ S_1 and S_0 status signals can identify various operations, but they are rarely used in small systems.
     - ✓

S_1	S_0	**Mode**
0	0	HLT
0	1	WRITE
1	0	READ
1	1	OPCODE FETCH

  3) IO/M' (pin 34)
     - ✓ This is a status signal used to differentiate I/O and memory operation

- ✓ When it is high, it indicates an I/O operation
- ✓ When it is low, it indicates a memory operation
- ✓ This signal is combined with RD' and WR' to generate I/O & memory control signals

- To indicate beginning of operation
  - One Special Signal called ALE (Address Latch Enable-Pin 30)
  - This is positive going pulse generated every time the 8085 begins an operation (machine cycle)
  - It indicates that the bits on AD7-AD0 are address bits
  - This signal is used primarily to latch the low-address from multiplexed bus & generate a separate set of address lines A7-A0.

4) Power Supply & Frequency Signal

- V_{cc} Pin no. 40, +5V Supply
- V_{ss} Pin no.20, Ground Reference
- X1, X2 Pin no.1 & 2, Crystal Oscillator is connected at these two pins. The frequency is internally divided by two; Therefore, to operate a system at 3MHz, the crystal should have a frequency of 6MHz.
- CLK (OUT) ☐Clock output. Pin No.37: This signal can be used as the system clock for other devices.

5) Externally Initiated Signals including Interrupts

- INTR (Input) ☐Interrupt Request. It is used as general purpose interrupt
- INTA' (Output) ☐Interrupt Acknowledge. It is used to acknowledge an interrupt.
- RST7.5, RST6.5, RST5.5 (Input) ☐Restart Interrupts.
  - These are vector interrupts that transfer the program control to specific memory locations.
  - They have higher priorities than INTR interrupt.
  - Among these 3 interrupts, the priority order is RST7.5, RST6.5, RST5.5
- TRAP (Input) ☐This is a non maskable interrupt & has the highest priority.
- HOLD (Input) ☐This signal indicates that a peripheral such as DMA Controller is requesting the use of address & data buses
- HLDA (Output) ☐Hold Acknowledge. This signal acknowledges the HOLD request
- READY (Input) ☐This signal is used to delay the microprocessor read or write cycles until as low- responding peripheral is ready to send or accept data. When the signal goes low, the microprocessor waits for an integral no. of clock cycles until it goes high.
- RESET IN' (Input) ☐When the signal on this pin goes low, the Program Counter is set to zero, the buses are tri-stated & microprocessor is reset.
- RESET OUT (Output) ☐This signal indicates that microprocessor is being

reset. The signal can be used to reset other devices.

6) Serial I/O Ports

- Two pins for serial transmission
  1) SID (Serial Input Data-pin 5)
  2) SOD (Serial Output Data-pin 4)
- In serial transmission, data bits are sent over a single line, one bit at a time.